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FPGA timing control for CMOS pixel characterization.

AUTHORS

Alessandro Michel Brunetti, Soheil Nazari, François Kinet, Alessandro Spinosi

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A Reconfigurable 10 ns Resolution, Wide Range FPGA-Based Timing Generator for CMOS Image Sensors

1st Alessandro Michel Brunetti^{1,2}

1: *iQrypto*

Boulevard Dolez, 31
7000 Mons, Belgium

2: *University of Mons,*
Boulevard Dolez, 31
7000 Mons, Belgium

a.brunetti@iqrypto.com

ORCID: 0000-0001-7429-9525

2nd Soheil Nazari^{1,2}

1: *iQrypto*

Boulevard Dolez, 31
7000 Mons, Belgium

2: *University of Mons,*
Boulevard Dolez, 31
7000 Mons, Belgium

s.nazari@iqrypto.com

3rd François Kinet¹

1: *iQrypto*

Boulevard Dolez, 31
7000 Mons, Belgium

f.kinet@iqrypto.com

4th Alessandro Spinosi¹

1: *iQrypto*

Boulevard Dolez, 31
7000 Mons, Belgium

a.spinosi@iqrypto.com

Abstract—CMOS image sensors are now ubiquitous across automotive, security, consumer and scientific markets. CMOS pixels, are sensitive to timing variations, thereby highlighting the need to carefully characterize their performance. In this context, reconfigurable architectures such as FPGA-based systems, offer a solid and flexible electronic platform to design the needed timing wave forms for pixel characterization. In a typical 4T pixel architecture, the transfer gate transistor is most sensitive to variations in rise/fall time edges and voltage because of the charge transfer mechanisms needed to transfer the charge from the photodiode to the floating diffusion. The ability to correctly set up the pulse's duration and resolution is therefore crucial for precise measurement of pixel parameters. In this paper, we use a simple three-register reconfigurable architecture that modulates the pixel control signal timings. Experimental results demonstrate that by using a commercial Xilinx Zynq-7020 architecture it is possible to reach a 10 ns resolution while keeping a reconfigurable timing up to almost 43 s for precise characterization of the CMOS pixels. Such approach is particularly useful for characterizing transfer gate signals and the sensor dark current where the combination of precision and long exposure times is needed.

Keywords — *FPGA, CMOS, Pixels, reconfigurable, characterization, sensors*

I. INTRODUCTION

CMOS Image Sensors are extremely popular for their low cost [1] and employed in a variety of applications such as automotive, security, consumer, surveillance amongst others [2]. Sensor performance continues to improve rapidly [3] due to the many scientific contributions advancing the state of the art both at global sensor level [4] or on specific areas such as pixel design [5][6], layout [7] and on the process engineering side [8]. Many of the scientific publications, however, have shown that CMOS pixels exhibit high sensitivity to the quality of the signals that are provided to the sensors, resulting in an overall degradation of the image sensor performance. This is particularly relevant for the transfer gate transistor [9][10] where charge transfer mechanisms dominate pixel performance. Tran *et al.* reported

an in-pixel circuit to generate 10 ns pulses [11] whose circuitry is present on-chip. In other approaches dedicated voltage controls have also gained popularity for CMOS image sensor applications due to their stability and precision [12]. While precise voltage control is important, in this work we are focusing on the time waveform aspect of the characterization where existing approaches suffer from limited reconfigurability.

In fact, one key device requiring highly reconfigurable timing and voltage is the 4T pixel, where the transfer gate transistor is sensitive to timing and voltage variations [13]. Monolithic on-chip solutions achieving nanosecond [14] or sub nanosecond timings are investigated [15] for fast imaging applications, however, they lack the necessary reconfiguration capability needed for characterization. In this sense, FPGA-based architectures offer reconfigurable capabilities to provide precise timing controls to drive the gates externally providing the flexibility needed for characterization and operation purposes. Several publications in the literature are shown to use nanosecond precision which is a necessity for a variety of fields [16][17]. Nevertheless, existing approaches are typically not able to provide a high dynamic range of timing precision.

For these reasons, in this paper, we propose a simple three-register FPGA-based reconfigurable architecture that precisely modulates pixel control signals such as the transfer gate and the reset transistor. We propose using a commercially available FPGA architecture providing 10 ns timing precision to characterize the pixel operation while being able to deliver a maximum time duration of almost 43 s. The presented paper is structured as follows: Section II introduces the CMOS pixels and their constraints, including a detailed analysis of the timing operation, Section III presents the methodology with the analysis of FPGA architecture, Section IV shows the measurement results and the measured reconfigurability capability of the presented methodology, and Section V finally concludes the paper.

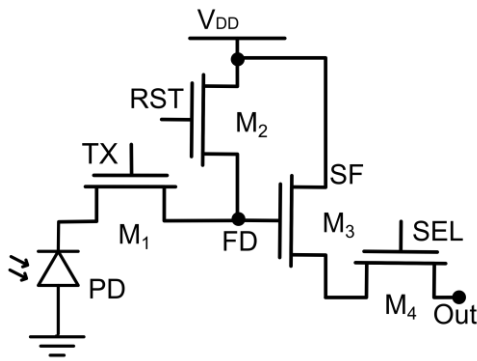


Fig.1. A typical 4T CMOS pixel schematic.

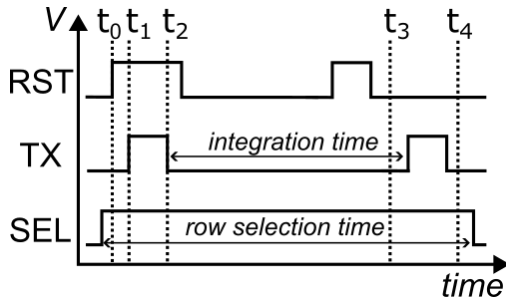


Fig.2. 4T CMOS pixel timing operation with correlated double sampling.

II. 4T CMOS PIXEL

For the purpose of this article we present a classical 4T architecture typical of rolling shutter operation of CMOS image sensors, nevertheless the considerations deriving from these conclusions can further be extended to other architectures and applications needing a similar level of precision in terms timing resolution.

A. 4T CMOS Pixel Schematic

A 4T CMOS pixel, as the name mentions, is made of 4 transistors with different functions. Figure 1 shows a typical 4T CMOS architecture. In this pixel, M_1 is the Transfer Gate transistor (TX), M_2 is the Reset Transistor (RST), M_3 is the Source Follower (SF) and M_4 is the Select transistor (SEL), V_{DD} is the supply voltage, PD is the pinned Photodiode, FD is the Floating Diffusion, and Out is the output to the column readout. Typically, the M_1 transistor control is extremely important because it determines the transfer of charge to the FD. The doping concentration of the PD and of the FD affect the overall pixel performance of parameters such as the Full Well Capacity and the Conversion Gain. Let us delve into the details of the pixel operation in the next paragraph.

B. 4T CMOS Pixel Operation

The pixel operation is relatively simple, the light is converted into charge that must be integrated over a certain period of time defined as “*integration time*”. To this objective, the temporal organisation of the signals is important and described in Figure 2 which shows a typical pixel operation where on the x-axis the time is reported and on the y-axis, voltage (V) is reported. The three signals controlling the respective MOSFETs are shown as RST, TX and SEL. Pixels are commonly organised in a matrix fashion and a line must be selected first which is often done by setting the SEL line high first. The SEL line remains high during the entire row readout time and we have defined it as the row selection time. It is possible to describe the correlated double sampling pixel

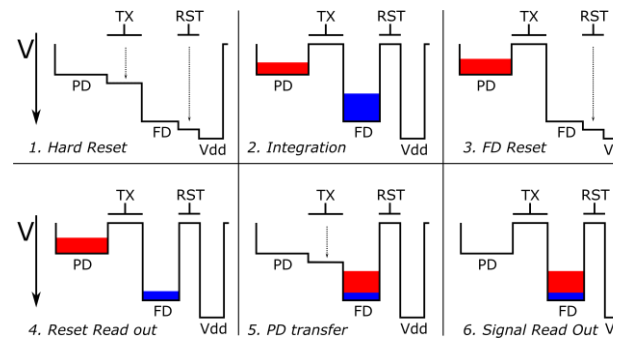


Fig. 3. 4T CMOS correlated double sampling pixel operation with potential diagrams.

operation in six steps. At the time t_0 , the RST signal goes high before the TX, this is to make sure that at the time t_1 , when the TX is goes high, the FD node is connected to V_{DD} if we neglect the V_{DS} in saturation of the M_2 transistor, thereby resetting the PD (1. Hard Reset). At the time t_2 , the TX goes down, effectively disconnecting the PD from the rest of the circuit and the integration time can start (2. Integration). To reduce kTC noise, the pixel typically operates a correlated double sampling readout by reading twice the pixel. Before reading the PD integrated charge, RST goes high again to effectively reset the FD (3. FD Reset) just before time t_3 where the RST signal on the FD is read in the column containing the reset charge with kTC noise (4. Reset Read out). Then TX can finally go high to enable the charge transfer of the photogenerated collected charge in PD to the FD (5. PD transfer) thereby enabling the signal plus kTC charge readout through the column (6. Signal Read out). Figure 3 describes the six phases of the 4T correlated double sampling pixel readout operation by highlighting the potential voltages in the PD diode, FD, and the RST and TX transistors. The useful photogenerated charge is represented in red, while the FD kTC noise charge is represented in blue. The voltage level of the PD is typically lower than the one of the FD because of a lower doping concentration of the diffusion in order to enable a

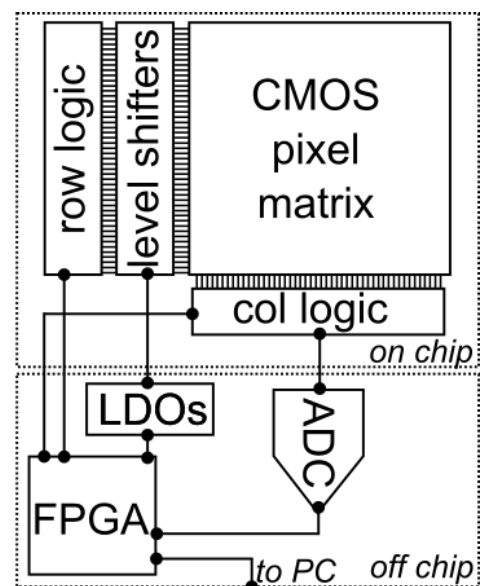


Fig. 4. Architecture set up of the CMOS pixel matrix control. The FPGA drives the Low Dropout Regulators (LDOs) off-chip that can drive level shifters and row logic inside the chip.

smoother transfer of charge. Several articles are published in the literature highlighting the influence of voltage levels on the charge transfer process on the FD. Pixel timings are crucial for correct device operation, and minimizing wasted delays between one cycle and the next results in overall faster readout time which enables pixels and sensors to operate at higher frames-per-second (fps). In the next section the pixel timing control methodology is presented.

III. METHODOLOGY

As CMOS pixels are frequently embedded in a more complex integrated circuit, to directly control the signal voltages and timings from external hardware, it is crucial to define an architecture where each of the necessary signals can be driven independently. Figure 4 shows the architecture used in this work, where the row and column logic are on chip controlled by an external FPGA. In this work, we are using a Xilinx Zynq-7020. Inside the FPGA, the building block of the timing control is defined as a simple 3-register structure that can control the timings with a 32-bit resolution. While this structure is implemented for each of the needed chip signals, in this work we will solely focus on the timings needed to operate the RST and TX transistors which are the most sensitive to timing and voltage variations. Figure 5 highlights the definition of the timings associated with the controls of one signal, for example the TX timing. The first register controls the timing from t_0 to the high transition, and it is defined as “*delay register*”, the second register controls the timing from the high transition to the low transition and is called “*high register*” register because during this period the signal is high. Finally, the third register controls the timing between the low transition to the next cyclical iteration, and it is called “*low register*”. A Finite State Machine (FSM) coordinates the registers in combination with a synchronization block. The combined output signal is then shared externally to the chip row logic. The advantage of using these registers is that they are completely reprogrammable during the chip operation thanks to the Command Line Interface (CLI) available through the FPGA. The timing loop is cyclical and can be changed at runtime. Because the FPGA FSM timing clock is 100 MHz, the theoretical associated timing resolution of the counter registers is 10 ns and the maximum counter value is proportional to 10 ns multiplied 2^{32} which returns a maximum value of $\sim 42,95$ s for each of the counters. With this approach, the maximum value is directly in trade-off with the minimum resolution and the FPGA FSM

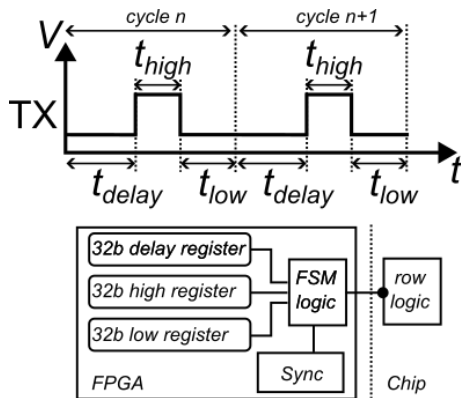


Fig. 5. FPGA-based three-register control structure for the TX transistor divided in three main counters: delay, high, low (D, H, L). A synchronized FSM combines the signals to keep the loop sent to the CMOS chip row logic.

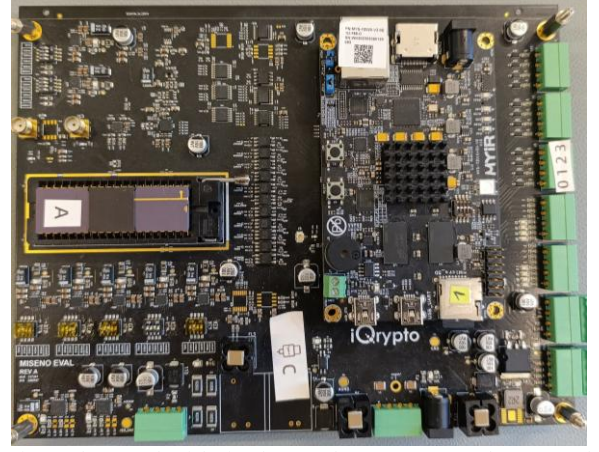


Fig. 6. Photograph of the implemented PCB to execute the proposed approach for TX, RST, and dark current measurements.

clock speed, however, for the typical imaging requirements, where CMOS image sensors operate at several fps, the maximum value is purely reserved to characterization operations such as dark current measurements where the charge must be integrated over longer periods of time and hence, the *integration time* can be set to longer periods.

To validate the methodology, we change the value of the registers through the CLI and measure the output to the CMOS image sensor chip pin where the TX and RST signals are expected to show the timing control capabilities of the approach. Figure 6 shows the physical implementation of the FPGA-based PCB board driving the ceramic packaged CMOS sensor at the center left of the board. Measurement results are reported in the next section.

IV. MEASUREMENTS

The registers delay, high and low are synthetically represented as D, H, and L and are configurable with bit numbers from 1 to 2^{32} with the limitation that the sum of every value is less or equal than 2^{32} , a LSB representing 10 ns. In the case of the values D=1, H=1, and L=1 the pulse period is 30 ns, and it can be shortened by using 0 values instead. For example, by setting D=0, a 50 % duty cycle is obtained, thereby generating a 50 MHz pixel clock cycle. Figure 7 shows the measurement results of the output signal applied to the load. In this case, three different control windows are presented where the bits are set to 1, 2 and 3 respectively for each of the control registers. In the right part of the figure, the measured output signal is plotted. Here, We observe the load dependent rise and fall time of the signals which respectively have a time constant τ of 7.8 ns and 5.4 ns, thereby translating in a maximum Voltage of 2.69 V for the shortest pulse duration, with a power supply of 3.3 V. In the case of 20 ns timing (H=2) the pulse shape already reaches 3.04 V of maximum value, and with 30 ns shape (H=3) the maximum Voltage reached is 3.26 V which is relatively settled.

Table 1 provides a summary of the measurement results highlighting a limitation of the driving strength compared to the device load: For the shortest possible timing (1 bit input),

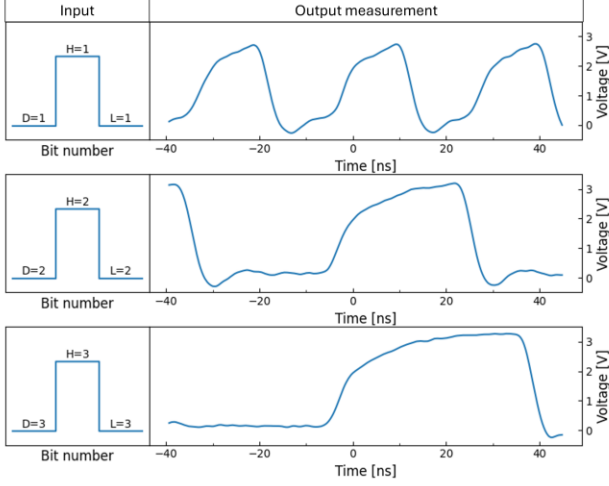


Fig. 7. Transfer gate pulse timing measurement result. On the left, the programmed bit values (1,2 and 3) on the right the measured output pulses of 10 ns, 20 ns, and 30 ns respectively. The target voltage level is 3.3V.

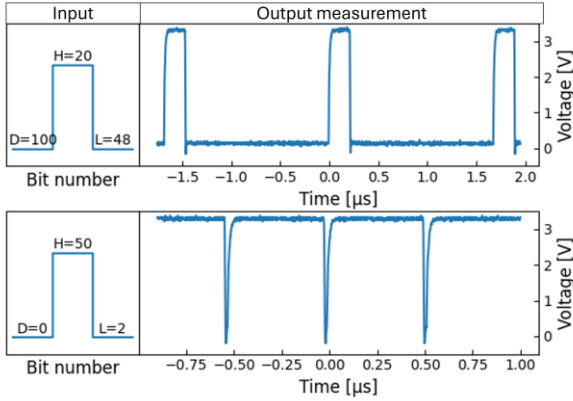


Fig. 8. Transfer gate asymmetrical timing input measurement result. On the left, the programmed bit values on the right the measured output. This figure shows the high reconfigurability. The target voltage level is 3.3V.

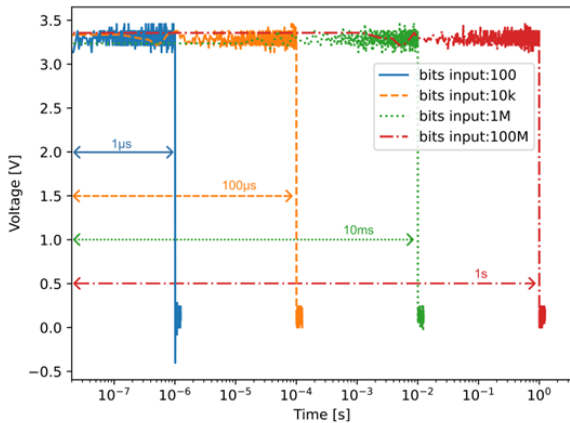


Fig. 9. Long pulse time measurement results displayed in semi-log for input bit values of 100 (blue), 10 K (orange), 1 M (green), and 100 M (red) showing the respective time pulse duration. The target voltage level is 3.3V.

the signal does not manage to rise to the target voltage. This means that the solution we present may not be suitable for ultra-short timing usage. However, for higher bit input we manage to get to the target voltage while preserving the

TABLE I. MEASURED VALUES

Parameter	Value
Time resolution min-max	10 ns-42.95 s
τ time constant rise with load	7.8 ns
τ time constant fall with load	5.4 ns
Max voltage with 10ns resolution peak	2.69 V

precision of 10 ns. Figure 8 shows the same measurement as in Figure 7 with asymmetrical bit input ($D \neq H \neq L$) highlighting the high level of flexibility of the proposed approach.

Figure 9 shows the reconfigurability capability for a wider range of input bits, logarithmically spaced and with H values of 100, 10 K, 1 M, and 100 M respectively, highlighting the high-dynamic range of the approach. These are plotted on log axis showing that with this approach a 3.3 V supply is settled for several timings. In the Figure, for visualization, only four results are reported, however, the principles apply to a wider range of timing signals (up to 42,95 s), thereby demonstrating that the proposed approach is a valid, simple and effective way to control pixel timings with the precision and high reconfigurability that is needed in CMOS pixels.

The experimental results confirm that the proposed reconfigurable timing engine can generate deterministic pulses with 10 ns resolution across its entire dynamic range. Such fine-grain control is pivotal for sensor-level tasks that hinge on precise transistor gating. EMVA1288 standard [18] carefully defines the procedures and times needed for characterization (i.e. signal and time resolutions) for standard image sensor characterization. The proposed methodology for example enables dark-current characterization with arbitrarily long integration windows, allowing accumulation of sufficient charge conditions without sacrificing temporal accuracy. In fact, the dark current is often boosted by increasing the temperature or the sensor gain, to measure meaningful signals. A higher integration time enables charge accumulation at room temperature. Likewise, for Photon Transfer Curve (PTC) analysis [19], the nanosecond-level timing lets adjust the transfer-gate window to the exact duration that optimizes charge-transfer mechanisms, thereby yielding cleaner measurements. The combination of high temporal resolution and extended range thus translates directly into faster, more reliable calibration of image-sensor pixels and, by extension, better optimization of imaging systems in real-world cameras, scientific instruments and time-sensitive device operation.

V. CONCLUSIONS

In this paper we first introduced the context of the need of precise timing operation in 4T CMOS image sensors. Such a need is mainly justified by the sensitivity of the transfer gate and the reset transistor in combination with the need of having long exposure times for dark current characterization times. In addition, achieving precise timing, enables an overall imager faster readout time which, in turn, translates into a higher fps capability of the CMOS sensor. The approach uses a commercial off-the-shelf hardware Xilinx Zynq-7020 FPGA to deliver the right combination of timings. The minimum resolvable timing is 10ns mainly limited by the 100 MHz FSM clock while delivering a maximum timing window duration of almost 43 s. The proposed architecture only utilizes three 32 b

registers per transistor control that are externally programmable at run time through the CLI. Measurement results show that the proposed methodology correctly delivers a reconfigurable pulse with a minimum resolution of 10 ns limited by the FPGA FSM and the device load while enabling a large range of reconfigurable timing by programming the three registers. In the context of device characterization, having an easy and highly reconfigurable device with 10ns precision in large timing windows expandable to 42,95 s enables the precise measurements that are needed for PTC and EMVA1288. Hence physical quantities such as dark current can be measured with normal gain at room. In conclusion, we proved that the proposed approach of a reconfigurable and simple method to control CMOS pixel transistors is effective both for runtime operation and for device characterization.

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